mikroprojekt

KONDOR AX

Advanced System Development Board

COMMS DEMO REFERENCE DESIGN GUIDE

UM0033

Rev. 1.0

2.11.2015.

Table of contents

Revision History

Revision	Date	Author	Modification
1.0	2.11.2015.	AS	Initial

Related Documents

ID	Code	Description
1	UM0026	KONDOR AX – User Manual
2	UM0032	KONDOR AX – Comms Demo Guide

1 Introduction

This document provides technical information and instructions for using the Comms Demo Reference Design for the KONDOR AX - Advanced System Development Board.

The Comms Demo Reference Design combines the Freescale i.MX6 Solo processor and Lattice ECP5 FPGA with Lattice CPRI and JESD204B IP cores to demo the capabilities of the KONDOR AX communications interfaces.

The project files in this demo run in **Diamond 3.5.1.**

This document provides FPGA circuit description. For more information on demo running instructions, as well as instructions for connecting the boards and necessary peripherals, consult the KONDOR AX – Comms Demo Guide document. For pinouts and other board specific information consult the KONDOR AX Board – User's Manual.

In addition to this user's guide the Comms Demo comes with the following:

- Verilog source code for the FPGA design
- Lattice Diamond software implementation project file
- Bitstream (in *.bit format)
- Kondor AX Advanced System Development Board User's Manual
- Comms Demo Guide document

Hardware requirements for the Comms Demo design:

- 2x Kondor AX Development Board with Lattice LFE5UM-85F FPGA device
- 2x 12V DC power supply for the Kondor AX Board
- Texas Instruments DAC37J82 EVM (DAC3XJ8X EVM)
- Texas Instruments ADS42JB69 EVM
- 2x 5V DC power supply for TI boards
- SMA cable for analog loopback
- 2x Finisar's FTLF1326P3BTL CPRI SFP+ transceivers
- 1x LC/LC Duplex 9/125 Single mode Fiber Optic Cable (DK-2933-01) for CPRI loopback

Software application and driver requirements:

- Lattice Diamond 3.5
- Micro-USB cable for programming the FPGA bitstream
- Diamond Programmer

1.1 Directory structure

The Comms Demo Reference Design is organized in several folders, as shown in Figure 1.

Figure 1. Comms Demo Reference Design directory structure

The 'Clarity' folder contains IP cores instantiated in Clarity.

The 'dia' folder contains the Diamond project files (.ldf, .lpf), implementation files and other related files.

The 'mico32' folder contains the Lattice Mico System files for the Lattice Mico32 soft processor core used in the design.

The ‘rtl’ folder contains the Verilog source code files.

The ‘wishsys’ folder contains Lattice Mico System files for the Wishbone interconnect.

2 Functional description

2.1 Overview

The codenames of the designs for the Comms Reference Demo are:

- RD0021_Kondor_AX_CommsDemo_DAC,
- RD0022_Kondor_AX_CommsDemo_ADC.

For this demo, two Kondor AX Development boards are required. One board is connected to the TI DAC37J82 EVM and programmed with the RD0021_Kondor_AX_CommsDemo_DAC design and the other is connected to the TI ADS42JB69 EVM over the FMC connector and programmed with the RD0022_Kondor_AX_CommsDemo_ADC design. The CPRI interface is connected to the Kondor's onboard SFP cage, while the JESD204B interface is driven to the onboard FMC connector.

There are two modes of operation of the Comms demo, the normal and the bridge mode. In the normal mode, JESD204B and CPRI interface are used independently. In the bridge mode, CPRI data is bridged to the JESD204B interface.

In the normal mode, JESD204B interface is used in the following manner. Software running on the i.MX6 processor on the Kondor AX board 1 generates stimulus data that's transferred to the ECP5 FPGA over the EIM interface and is outputted by JESD204B TX IP core. JESD204B interface is driven to the onboard FMC connector, where TI DAC37J82 EVM FMC add-on card is plugged in. DAC37J82 EVM is cable connected with the TI ADS42JB69 EVM add-on card plugged into the Kondor AX board 2 FMC connector. JESD204B data received from ADS42JB69 EVM on the second board is driven back to the data_framer core where it's read by the i.MX6 over the EIM interface and checked if the waveform of the received data is consistent with the originally generated data.

In normal mode, each of the boards for the CPRI interface utilizes a Data generator and a Data checker core inside FPGA fabric and send each other identical data to check if the CPRI link is operational and if the data is transferred correctly. CPRI SFP transceivers on both boards are connected via optical cable.

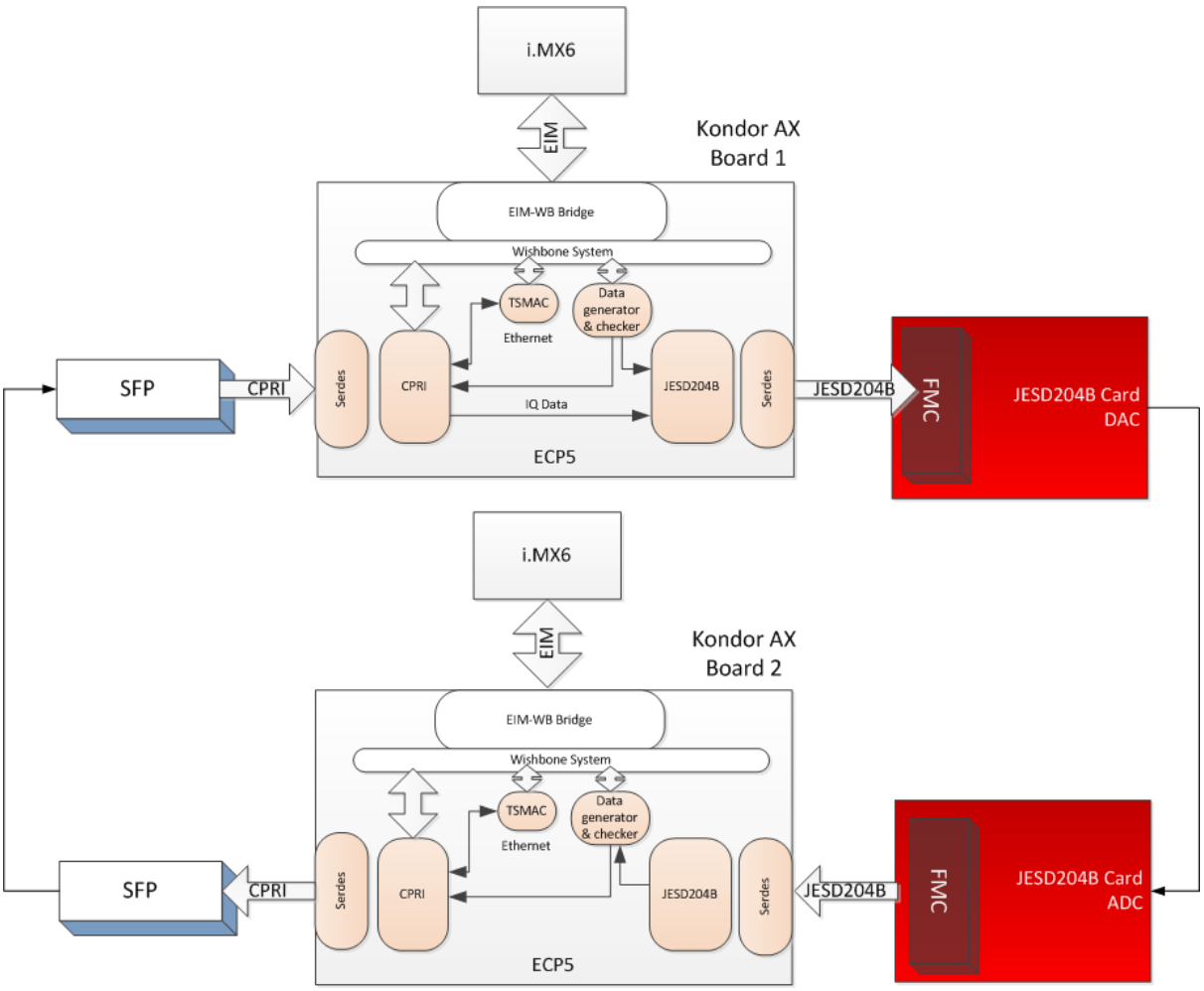

Figure 2. Comms Demo Reference Design block schematic

Bridge mode of the Comms demo is implemented in the following manner. i.MX6 of the Kondor AX board 2 generates data for transmission over CPRI. This data is received over CPRI on Kondor AX Board 1, bridged to the JESD204B and converted to analog domain via TI DAC board. Analog data is transferred to the TI ADC board, received over JESD240B interface on the Kondor AX board 2, and checked by the i.MX6.

i.MX6 processors on both boards communicate with each other over the Ethernet interface connected to the Lattice Tri-speed Ethernet MAC IP core over the EIM interface. Ethernet data is transferred between the boards using the control and management information flow of the CPRI link.

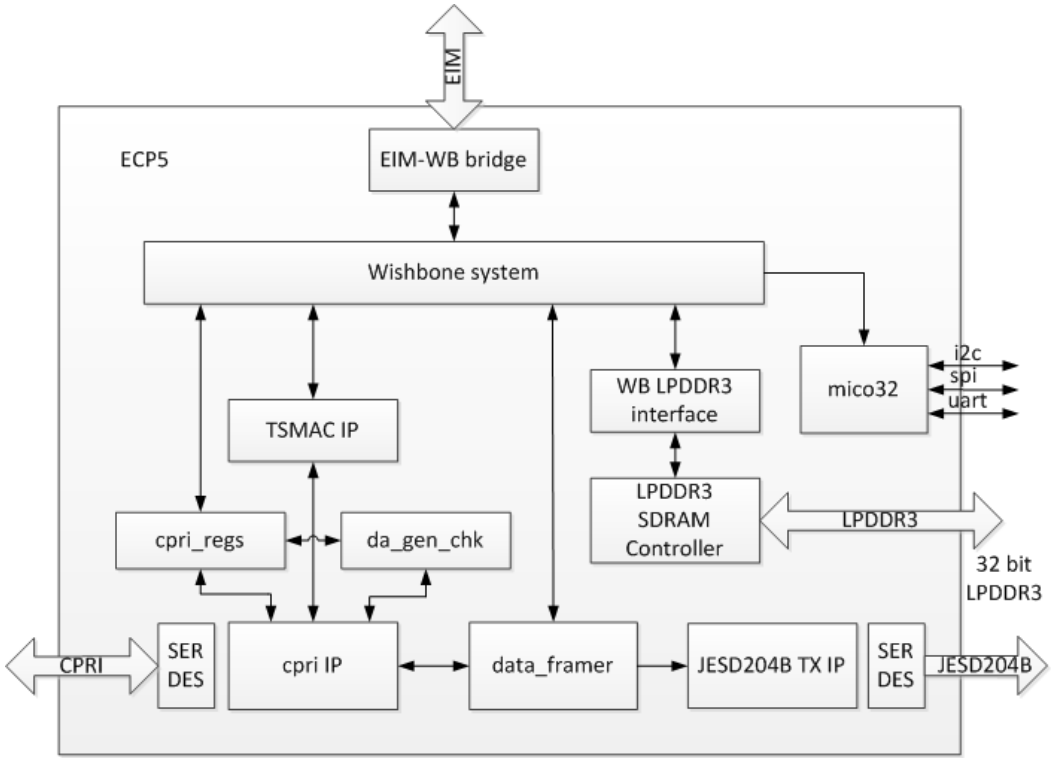

Figure 3. Comms Demo Reference Design DAC detailed Block Schematic

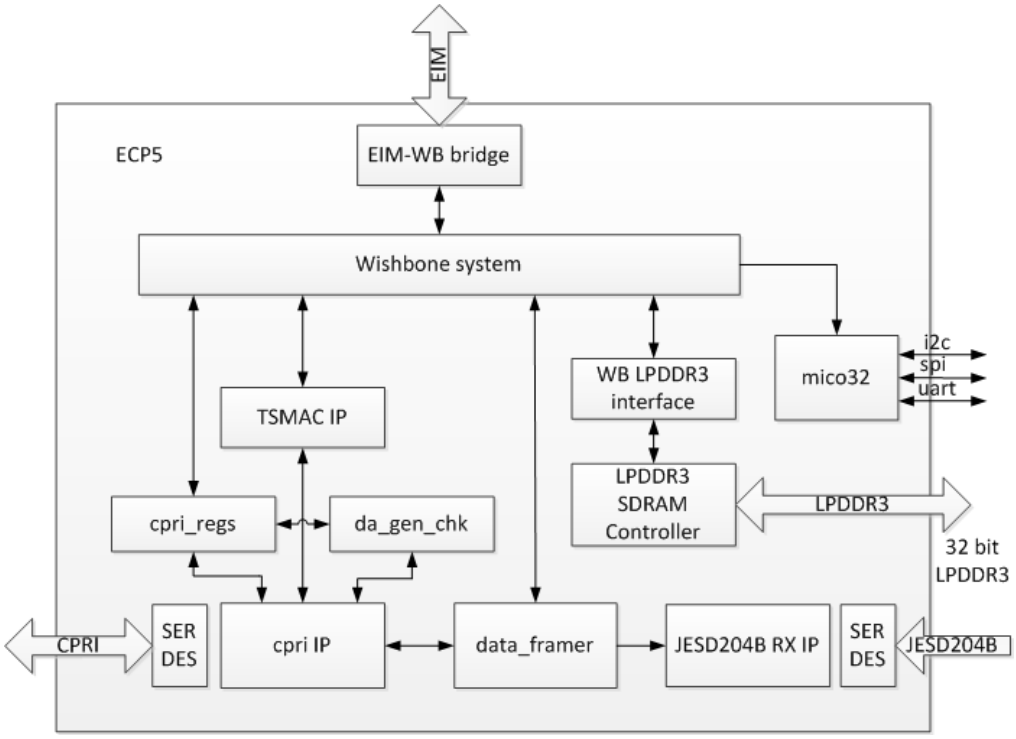

Figure 4. Comms Demo Reference Design ADC detailed Block Schematic

Table 1: Comms Demo Reference Design ports definition

Port	Width	I/0	Description 1/2
clk_in	1	In	100 MHz clock input
eim_clk	1	In	eim interface 50 MHz clock input
eim_addr	26	In	eim interface address
eim_lba	1	In	eim interface address valid signal, active low
eim_cs	2	In	eim interface chip select, active low
eim_oe	1	In	eim interface output enable, active low
eim_rw	1	In	eim write enable, active low indicates a write access
eim_be	4	In	eim interface byte enable
eim_data	32	In	eim interface data bus
eim_wait	1	Out	eim interface busy/wait signal, active low
em_ddr_data	32	In/out	Memory bidirectional data bus
em_ddr_dqs	4	Out	Memory bidirectional, differential pair data strobe
em_ddr_clk	1	Out	Up to 400 MHz differential pair memory clock generated by the controller
em_ddr_cke	1	Out	Memory clock enable generated by the controller
em_ddr_cs_n	1	Out	Memory chip select
em_ddr_odt	1	Out	Memory on-die termination control
em_ddr_dm	4	Out	LPDDR3 memory write data mask
em_ddr_ca	10	Out	Memory command and address bus
jesd_clk_p	1	In	JESD204B interface reference clock, positive differential pair
jesd_clk_n	1	In	JESD204B interface reference clock, negative differential pair
jesd_hdinp	2	In	JESD204B interface reference clock positive differential pair
jesd_hdinn	2	In	JESD204B interface reference clock negative differential pair
jesd_hdoutp	2	Out	JESD204B interface high-speed PCS/SERDES output, positive
jesd_hdoutn	2	Out	JESD204B interface high-speed PCS/SERDES output, negative
syncn_in	1	In	JESD204B TX interface synchronization signal, positive
syncn_in_n	1	In	JESD204B TX interface synchronization signal, negative
syncn_out	1	Out	JESD204B RX interface synchronization signal, positive
syncn_out_n	1	Out	JESD204B RX interface synchronization signal, negative
sysref	1	In	JESD204B interface timing signal, positive
sysref_n	1	In	JESD204B interface timing signal, negative
cpri_clk_p	1	In	CPRI interface reference clock positive differential pair
cpri_clk_n	1	In	CPRI interface reference clock negative differential pair
cpri_hdinp	1	In	CPRI interface high-speed PCS/SERDES input, positive
cpri_hdinn	1	In	CPRI interface high-speed PCS/SERDES input, negative
cpri_hdoutp	1	Out	CPRI interface high-speed PCS/SERDES output, positive
cpri_hdoutn	1	Out	CPRI interface high-speed PCS/SERDES output, negative
dac_spi_cs_0	1	Out	SPI chip select for DAC37J82
spi_muxed0	1	In/Out	SPI chip select for LMK04828 on DAC board, or SPI MISO from LMK04828 on ADC board
spi_muxed1	1	In/Out	SPI chip select for ADS42JB69, or SPI MISO from LMK04828 on DAC board
spi_muxed2	1	In/Out	SPI chip select for LMK04828 on ADC board, or SPI MISO from DAC37J82
spi_miso	1	In	SPI MISO from ADS42JB69
spi_mosi	1	Out	SPI MOSI
spi_clk	1	Out	SPI clock

Port	Width	I/O	Description 2/2
spi_dir_control	1	Out	SPI direction control
sfp2_tx_disable	1	Out	SFP transceiver transmit disable
uart_rx	1	In	Mico32 uart rx
uart_tx	1	Out	Mico32 uart tx
led_out	8	Out	LEDs
exp_conn	9	Out	J17 expansion connector

2.2 EIM interface

EIM (External Interface Module) is a general purpose parallel interface that enables embedded CPUs to control different types of external peripherals and memories.

The details of the EIM interface are described in chapter 22 of the i.MX6 reference manual. This EIM interface is configured to work in Synchronous write/read none multiplexed Operation mode. The transfers are clocked by a 50 MHz ARM-supplied clock (eim_clk). The EIM-WB bridge (iq_bridge_eim2wish.v) translates EIM into Wishbone requests.

2.3 Wishbone system interconnect

The EIM-WB bridge translates the EIM signals coming from the CPU to requests on the internal Wishbone bus. The internal Wishbone bus interconnect is generated using the Mico System builder. The bus uses 32-bit addresses and 32-bit data. Table 2 shows the address mappings of various peripherals connected to the Wishbone bus.

Table 2: Wishbone system interconnect peripheral addresses

Wishbone address	Peripheral
0xA0000000	CPRI registers
0xD0000000	Status and control registers
0xE0000000	Tri speed Ethernet MAC

2.4 JESD204B Interface

2.4.1 DAC

The Kondor AX board connected to the DAC37J82 board utilizes the design with the JESD204B TX IP core (RD0021_Kondor_AX_CommsDemo_DAC). The PCS DCU0 Channel 0 and Channel 1 locations on the chip are used. The JESD204B TX IP core is generated with the following parameters:

Table 3: JESD204B TX IP core parameters

JESD204B TX IP core parameters	Parameter value
LMF	222
K	9
CF	0
CS	0
HD	0
N	16
N'	16
M	2
S	1
Subclass	1

DAC37J82 input data rate is 122.88 MSPS, output data rate is 245.76 MSPS and SerDes line rate is 2.4576 Gbps. LMK04828 is configured to provide 245.76 MHz reference clock for FPGA JESD204B TX IP core which is divided inside FPGA to 122.88 MHz, and 245.76 MHz for DAC37J82.

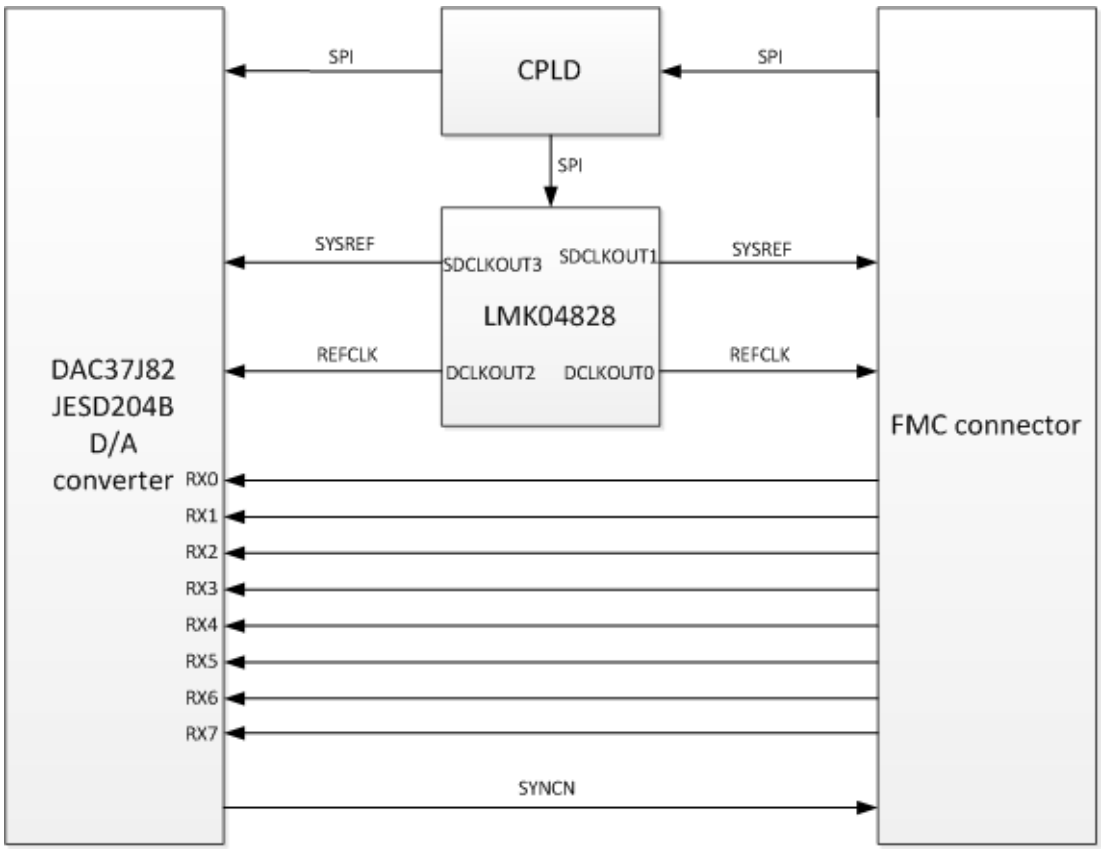

Figure 5. DAC37J82 board connection to FMC connector

Table 4: DAC37J82's FMC connector connection to ECP5

Signal	FMC connector	FPGA
jesd_clk_p	D4	AM14
jesd_clk_n	D5	AM15
jesd_hdoutp[0]	C2	AK9
jesd_hdoutn[0]	C3	AK10
jesd_hdoutp[1]	A22	AK12
jesd_hdoutn[1]	A23	AK13
sysref_p	G9	AC30
sysref_n	G10	AB31
syncn_in_p	F10	W31
syncn_in_n	F11	Y32
spi_cs_dac	D15	AK30
spi_cs_lmk	G15	L29
spi_clk	C14	K28
spi_miso_dac	G16	L26
spi_miso_lmk	H16	L30
spi_mosi	C15	L27
spi_dir_control	H17	K29

2.4.2 ADC

The Kondor AX board connected to the ADS42JB69 board utilizes the design with the JESD204B RX IP core (RD0022_Kondor_AX_CommsDemo_ADC). The PCS DCU0 Channel 0 location on the chip is used. The JESD204B RX IP core is generated with the following parameters:

Table 5: JESD204B RX IP core parameters

JESD204B RX IP core parameters	Parameter value
LMF	122
K	20
CF	0
CS	0
HD	0
N	16
N'	16
M	2
S	1
Subclass	1

The ADS42JB69 is configured in 2-Lane (20x) SerDes mode, but only one lane is received by the FPGA because the other lane of the ADS42JB69 is connected to DCU1 channel 0 of the FPGA that's utilized for CPRI interface. LMK04828 is configured to provide 122.88 MHz reference clock for FPGA JESD204B RX IP core and for the ADS42JB69. SerDes line rate is 2457.6 Mbps.

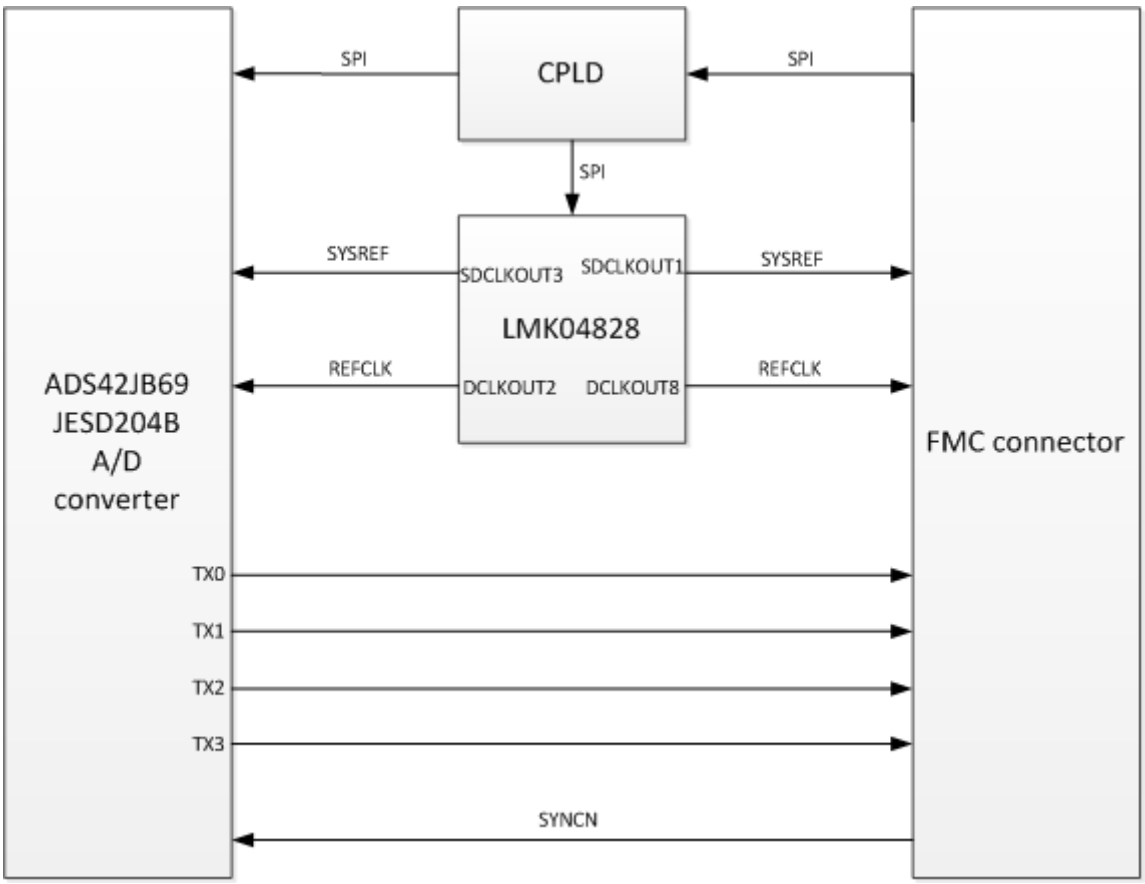

Figure 6. ADS42JB69 board connection to FMC connector

Table 6: ADC's FMC connector connection to ECP5

Signal	FMC connector	FPGA
jesd_clk_p	D4	AM14
jesd_clk_n	D5	AM15
jesd_hdinp	C6	AM8
jesd_hdinn	C7	AM9
sysref_p	G9	AC30
sysref_n	G10	AB31
syncn_out_p	G12	AB28
syncn_out_n	G13	AB27
spi_cs_adc	H16	L30
spi_cs_lmk	G16	L26
spi_clk	C14	K28
spi_miso_adc	D14	AG30
spi_miso_lmk	G15	L29
spi_mosi	C15	L27
spi_dir_control	H17	K29

2.5 CPRI interface

CPRI portion of the Comms Demo Reference design focuses on the ability of CPRI to transfer multiple data layers, i.e. parallel IQ data, serial HDLC and Ethernet data, parallel vendor specific data and L1 Inband Protocol information.

The transmit IQ data can be driven either from a Data generator core in the FPGA fabric or data generated by i.MX6 processor (normal or bridged mode). Received CPRI data is driven to the Data checker core and can be driven directly to the JESD204B TX interface. This data generator circuitry, implemented in the FPGA fabric, consists of the clocking structure, pseudo-random number generators for the fast and slow C&M channels, as well as circuits which insert numbered words into the user IQ data and the vendor-specific channels. On the RX side of each board, the received data is passed to the data checker soft logic, with error counters connected to user registers for monitoring.

The C&M channel is encapsulated as Ethernet and connected to the Lattice Tri speed MAC IP core, which is handled by the i.MX6 over the EIM interface. CPRI IP Core is working in the Matched Rate MII mode, i.e. CPRI IP core provides a standard MII interface that is connected to the Ethernet MAC IP core.

The L1 Inband and HDLC signaling are available in the design for the user to expand the delivered demo.

The PCS DCU1 Channel 0 location on the chip is used for the CPRI interface. It has been generated in CPRI mode and supports rates of 1.228/2.457/3.072 Gbps. For the Comms Demo Reference Design, CPRI is configured to run at 2.4576 Gbps through SCI register interface. A Si5338 clock generator is used to provide the 122.88 MHz reference clock for the DCU1.

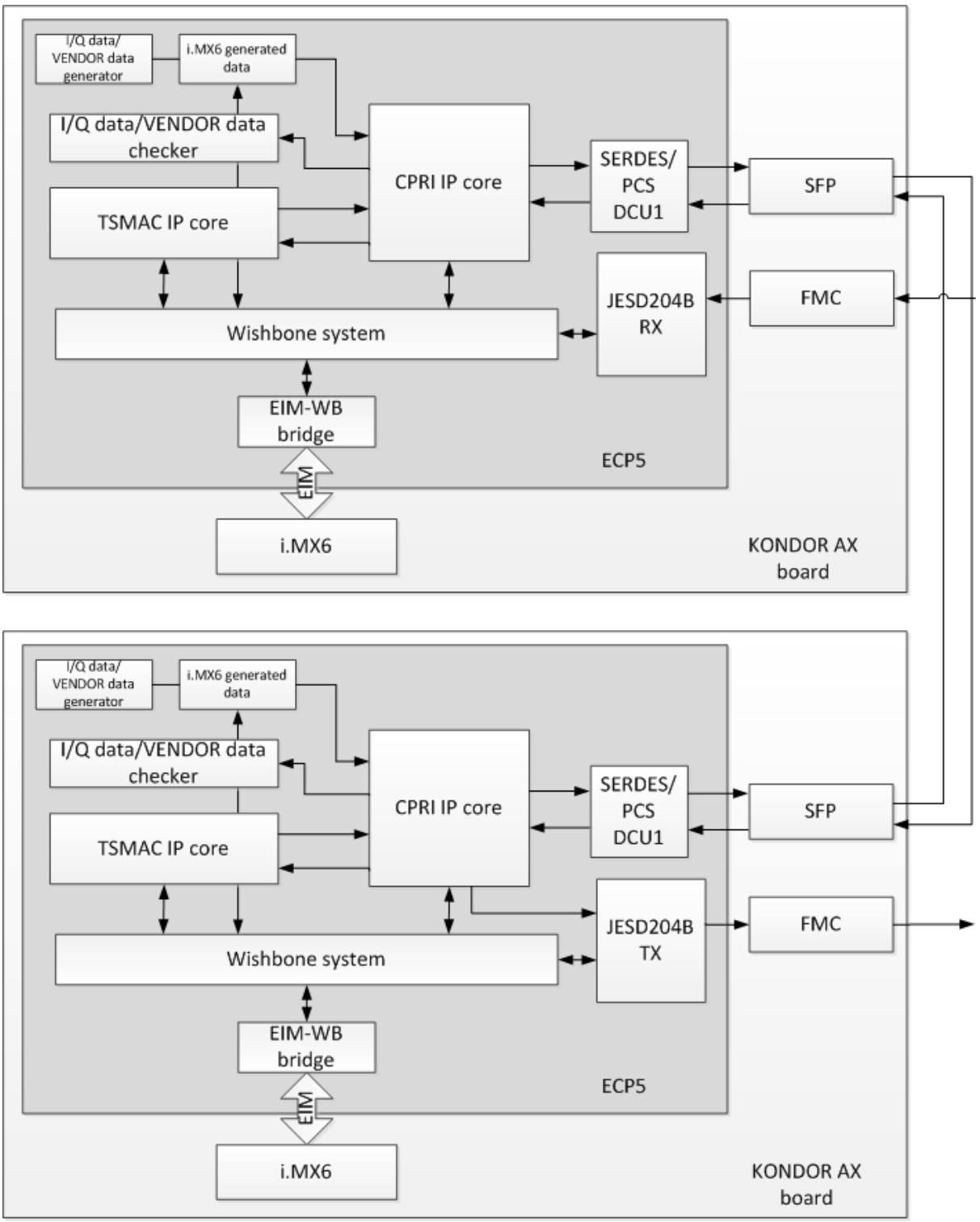

Figure 7. CPRI FPGA block schematic

2.6 Data framer core

Data framer core is used for controlling the data flow from/to JESD204B and CPRI interfaces and providing Wishbone register interface for the i.MX6 accessible through EIM_WB bridge. Control and status registers of the data framer core are described in the Table 7.

Table 7: Data framer control and status registers description

Register	Address	Width	Description 1/2
reg_0	0xD0000000	32	**[8:0]** number of samples written by i.MX6 to 0xD0010000 or 0xD0020000 locations **[29]** CPRI data flow control bit: 0 - data transmitted over CPRI interface is data generated in FPGA 1 - data transmitted over CPRI interface is data from 0xD0020000 locations **[30]** JESD204B TX data flow control bit: 0 - data transmitted to DAC board over JESD204b interface is data from 0xD0010000, 1 - data transmitted to DAC board over JESD204b interface is data received from CPRI interface **[31]** handshake control between i.MX6 and FPGA i.MX6 set this bit to 1 after all samples have been written to 0xD0010000 or 0xD0020000 locations and after the number of samples has been written to D0000000[8:0]
reg_1	0xD0000004	32	**[8:0]** number of samples received over JESD240b from ADC board FPGA should write to 0xD0010800 locations **[30]** handshake control between i.MX6 and FPGA 0 - FPGA is not done writing the samples to 0xD0010800 1 - FPGA sets this bit to 1 after it has written data samples received over JESD204B to 0xD0010800. At the same time FPGA clears the bit D0000004[31] **[31]** handshake control between i.MX6 and FPGA 1 - i.MX6 sets this bit to 1 when FPGA should start writing samples to 0xD0010800, FPGA clears it after it's done writing the samples

Register	Address	Width	Description 2/2
status_reg	0xD0000008	32	**[1:0]** - JESD204B RX (ADC) serdes disparity error **[3:2]** - JESD204B RX (ADC) serdes code violation error **[4]** - JESD204B RX (ADC) serdes loss of signal **[5]** - JESD204B RX (ADC) serdes cdr loss of lock **[6]** - all_aligned **[7]** - init_align_fail **[8]** - lane_align **[9]** - unexpect_ctrl **[10]** - cgs_err **[11]** - cfg_mismatch_err **[15:12]** - RFU **[17:16]** - JESD204B TX (DAC) state - 0 - CGS phase, 1 - ILAS phase, 2 - transmission of data, 3 - reset state **[23:18]** - RFU **[24]** - cpri_rx serdes disparity error **[25]** - cpri_rx serdes code violation error **[28:26]** - CPRI IP core state 1 - synchronization, 2 - protocol setup, 3 - c/m plane setup, 4 - interface and vendor negotiation, 5 - operation **[31:26]** - RFU
control_reg	0xD000000C		**[0]** - reinitialize dac and lmk over SPI **[1]** - reinitialize adc and lmk over SPI **[2]** - reset_cpri **[3]** - reset_dac **[4]** - reset_adc
bram_wr	0xD0010000 - 0xD00107FC	32	512 32-bit locations, i.MX6 writes samples here to be sent over JESD204B to DAC board
bram_rd	0xD0010800 - 0xD0010FFC	32	512 32-bit locations, FPGA writes samples here that have been received over JESD204B from ADC board
cpri_bram	0xD0020000 - 0xD00207FC	32	512 32-bit locations, i.MX6 writes samples here to be sent over CPRI interface

2.7 Mico32

Lattice Mico32 soft processor is used for:

- initializing Si5338 clock generator through I2C interface for the CPRI reference clock,
- initializing ADC and LMK04828 chips on ADS42JB69 EVM board through SPI interface,
- initializing DAC37J82 and LMK04828 chips on DAC37J82 EVM board through SPI interface.

Through a master_passthru port it also has access to CPRI IP core registers at the 0xA0000000 address.

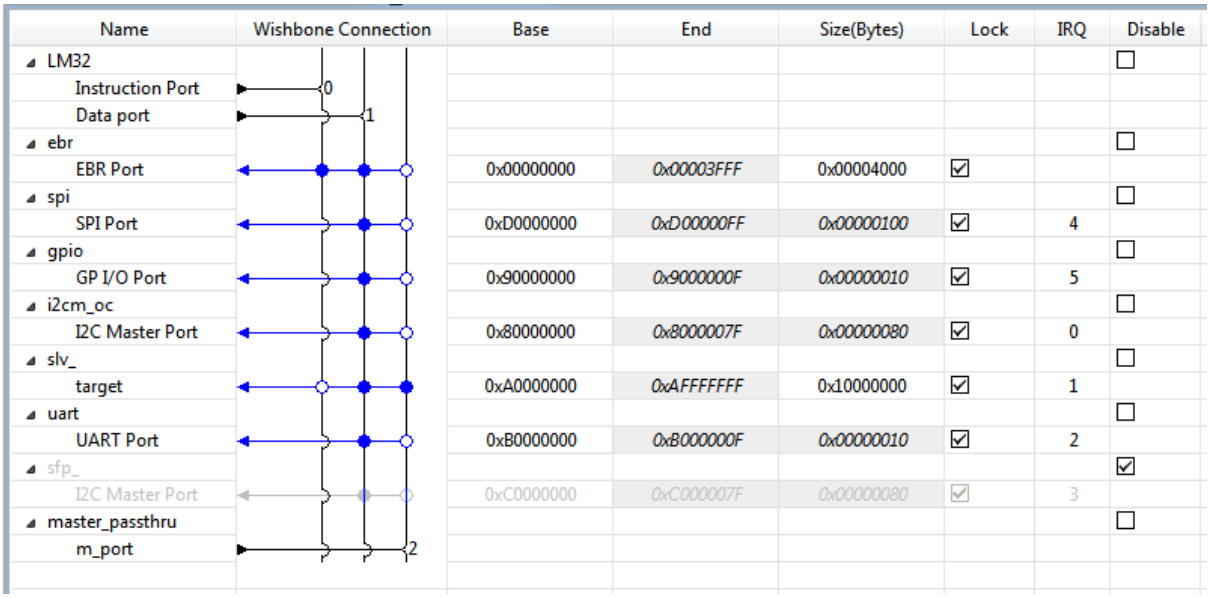

Figure 8. Mico32 configuration snapshot

2.8 Clocking

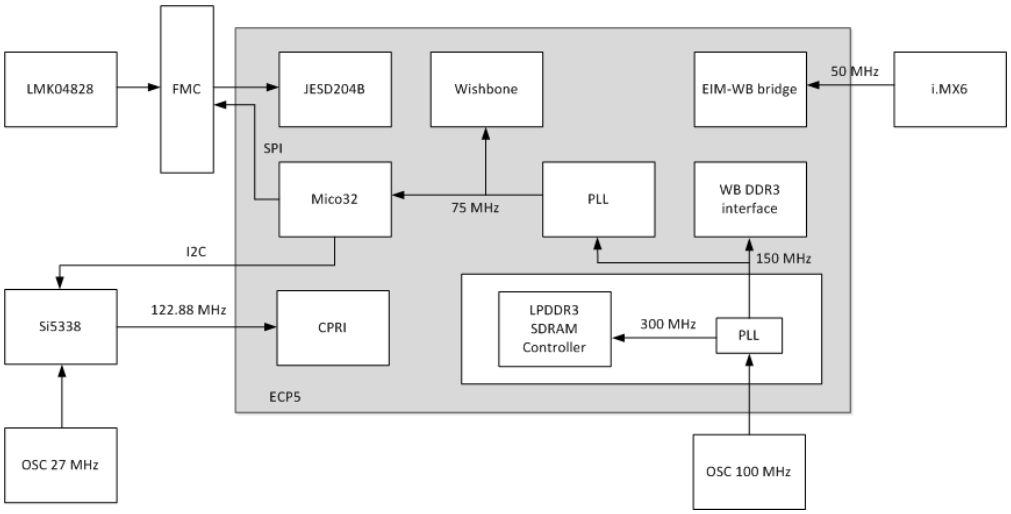

Figure 9. Comms Demo clocking scheme

The LPDDR3 SDRAM Controller uses its dedicated onboard 100 MHz reference clock (clk_in) to generate a 300 MHz clock for memory access and a 150 MHz system clock (sclk). The Wishbone DDR3 interface module runs on this 150 MHz system clock.

This 150 MHz system clock (sclk) is used as the input clock for a PLL which generates 75 MHz clock. The 75 MHz clock clocks the Wishbone bus. The PLL lock signal from this PLL is used as the reset for the Wishbone bus.

The 122.88 MHz differential reference clock for CPRI interface is generated by the Si5338 onboard PLL chip. Si5338 is configured over I2C by Lattice Mico32 soft processor.

JESD204B RX and TX interfaces are clocked by the LMK04828 clock generator through FMC connector. LMK04828 is configured over SPI by Lattice Mico32 soft processor.

The EIM interface transfers are clocked by a 50 MHz ARM-supplied clock (eim_clk).

The reset signal for the LPDDR3 SDRAM Controller (rstn) is generated by a 20-bit wide counter which is initialized on FPGA configuration and runs on a 77.5 MHz clock generated by an internal oscillator.

3 Design information

3.1 IP versions

Table 8: Comms Demo IP Core versions

IP Name	IP Version
LPDDR3 SDRAM Controller	1.0esr
CPRI	5.0
JESD204B	2.1
Dual Clock FIFO	5.8
RAM_DP	6.4
PLL	5.7
EXTREF	1.1

3.2 Resource Utilization

Table 9: Comms Demo Resource Utilization on ECP5

Design	Slices	LUTs	Registers	EBRs
RD0022_Kondor_AX_CommsDemo_ADC	13386	19008	14228	34
RD0021_Kondor_AX_CommsDemo_DAC	13347	18195	13158	35

4 Reference information

The following documents provide more information:

Lattice Semiconductors:

- DS1044 - ECP5 family datasheet
- TN1261 - ECP5 SERDES/PCS Usage guide
- TN1263 - ECP5 sysCLOCK PLL/DLL Design and Usage Guide
- TN1265 - ECP5 High-Speed I/O Interface
- IPUG56 - CPRI IP Core User's Guide
- IPUG74 - CPRI IP Core Low Latency Variation Design Considerations
- IPUG113 - JESD204B IP Core User's Guide
- IPUG51 - Tri-Speed Ethernet MAC User's Guide

- IPUG110 - LPDDR3 SDRAM Controller IP Core User's Guide

Texas Instruments:

- DAC37J82 Data Sheet
- DAC3XJ8XEVM User's Guide
- ADS42JB69 Data Sheet
- ADS42JB69EVM User's Guide

CPRI:

- CPRI Specification V3.0

Finisar:

- Finisar CPRI SFP+ Transceiver

JESD204B:

- JESD204B specification

Freescale

- IMX6SDLRM i.MX 6Solo/6DualLite Applications Processor Reference Manual

5 Ordering information

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- Instant Messaging Support
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